In the specification:

Please amend the paragraph on page 10, lines 9-17 as follows:

Memory device 1 may further include address logic 9, such as a row decoder circuit 9A, which receives an external address value and asserts a word line 7 and plate line 8 pair corresponding to the address value; and column decoder circuit 9B, which receives the address value and connects one or more bit lines 6 to data input/output bus 12 via data input/output block 11. The row address decode circuit 9A drives the word line 7 to a voltage level so as to connect bit lines 6 to capacitive elements of memory cells 3 in the selected row. This causes the charge appearing in each memory cell 3 in the selected row to be shared with the charge (such as a zero charge) appearing on the corresponding bit line 6, thereby changing the voltage appearing on the corresponding bit line 6 accordingly.

Please amend the paragraph on page 12, line 11 to page 13, line 2 as follows:

The control circuit 13 may receive as an input a test/normal input signal which, based on its value, configures the memory device 1 in the test mode of operation. When in the test mode, sense amplifiers 10 are disabled by the control circuit 13 or otherwise disconnected from bit lines 6 so as to be incapable of sensing voltage levels appearing thereon. This results in memory device 1 being capable of performing memory read operations that are modified for testing memory cells 3. As stated above, the control circuit 13 provides control for the operations of the memory device 1.

Precharge/equilibrate circuitry (not shown) may be controlled by the control circuit 13 so as to precharge the bit lines 6 to a predetermined voltage level, such as ground.

Please amend the paragraph on page 19, lines 3-13 as follows:

Next, the voltage level maintained by the memory cell 3 connected to the selected bit line 6 may be compared to a predetermined threshold voltage level (step 126) to determine if the memory cell 3 will be sufficiently usable over a prolonged period of time. In the case of the selected memory cell 3 storing a logic one data value and the voltage level being greater than the threshold voltage level, the tested memory cell 3 may be deemed to be operating at an acceptable level (marked at step 128). In the case of the selected memory cell 3 storing a logic zero data value and the voltage level being less than the threshold voltage level, the tested memory cell 3 may be deemed to be operating at an acceptable level. However, if the voltage level is below the predetermined threshold voltage level for logic one data values or above the predetermined threshold voltage level for logic zero data values, then the memory cell 3 may be marked as defective (step 130).

Please amend the paragraph on page 20, lines 1-10 as follows:

After a memory cell 3 has been tested, another bit line 6 may be selected (step 120) on the same row of memory cells by incrementing/decrementing the counter 28 by toggling test signal testclk. The output of counter 28 may be passed through the decode circuit 26 which in turn only activates another select transistor 24. Steps 114-118 are then repeated to test the memory cell 3 corresponding to the newly selected bit line 6.

Once all the memory cells 3 in the selected row have been tested (step 118), another row of memory cells 3 is selected to test the memory cells 3 therein (step 122). This process is repeated until all the memory cells 3 in the array 2 have been tested. Upon the completion of the testing operation, the memory cells 3 marked as unacceptable may be replaced by redundancy circuitry (not shown). Alternatively, the memory device 1 may be scrapped.